Your search matched **17** of **951805** documents.

A maximum of **17** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

FPGA and status Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **The LANL Neutron Science Center TOF/PSD module: status and pr gı**
Rose, C.R.; Hammonds, J.P.; Nelson, R.A.; Weizeorick, J.T.;
Real Time Conference, 1999. Santa Fe 1999. 11th IEEE NPSS , 14-18 June 199
Page(s): 137 -139

[Abstract] [PDF Full-Text (196 KB)] **IEEE CNF**

2 **A novel current control strategy for PWM inverters using the sliding ı techniques**
Rey, A.B.; de Pablo, S.; Ruiz, J.M.; Ravelo, J.A.;
Power Electronics Congress, 2000. CIEP 2000. VII IEEE International , 15-19 O 2000
Page(s): 276 -279

[Abstract] [PDF Full-Text (252 KB)] **IEEE CNF**

3 **Low power floating point MAFs-a comparative study**
Pillai, R.V.K.; Shah, S.Y.A.; Al-Khalili, A.J.; Al-Khalili, D.;
Signal Processing and its Applications, Sixth International, Symposium on. 200
Volume: 1 , 13-16 Aug. 2001
Page(s): 284 -287 vol.1

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

4 **A single chip implementati n f receive path terminati n f r SONET (and quadruple SONET OC-3c**
Seetharam, S.W.; Minden, G.J.; Evans, J.B.;

Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium o
Volume: 3 , 30 May-2 June 1994
Page(s): 237 -240 vol.3

[Abstract] [PDF Full-Text (412 KB)] **IEEE CNF**

5 **The design and implementation of a context switching FPGA**
Scalera, S.M.; Vazquez, J.R.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium o
17 April 1998
Page(s): 78 -85

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

6 **A CAD suite for high-performance FPGA design**
Hutchings, B.; Bellows, P.; Hawkins, J.; Hemmert, S.; Nelson, B.; Rytting, M.;
Field-Programmable Custom Computing Machines, 1999. FCCM '99. Proceeding:
Seventh Annual IEEE Symposium on , 21-23 April 1999
Page(s): 12 -24

[Abstract] [PDF Full-Text (188 KB)] **IEEE CNF**

7 **FPGA technology snapshot: current devices and design tools**
Krupnova, H.; Saucier, G.;
Rapid System Prototyping, 2000. RSP 2000. Proceedings. 11th International W
on , 21-23 June 2000
Page(s): 200 -205

[Abstract] [PDF Full-Text (128 KB)] **IEEE CNF**

8 **Prototyping of efficient hardware algorithms for data compression in future communication systems**
Mukherjee, A.; Motgi, N.; Becker, J.; Friebe, A.; Habermann, C.; Glesner, M.;
Rapid System Prototyping, 12th International Workshop on, 2001. , 25-27 June
Page(s): 58 -63

[Abstract] [PDF Full-Text (556 KB)] **IEEE CNF**

9 **SONOS nonv latile semiconductor memories for space and military applicati ns**
Adams, D.A.; Mavisz, D.; Murray, J.R.; White, M.H.;

Aerospace Conference, 2001, IEEE Proceedings. , Volume: 5 , 10-17 March 20(
Page(s): 2295 -2300 vol.5

[Abstract] [PDF Full-Text (692 KB)] **IEEE CNF**

10 **A 3D laser micro-sensor integrating control and data processing in a FPGA-based calculator**
Arana-Arejolaleiba, N.; Briot, M.; Ganibal, C.; Nketsa, A.; Prajoux, R.;
3-D Digital Imaging and Modeling, 2001. Proceedings. Third International Confe on , 28 May-1 June 2001
Page(s): 107 -114

[Abstract] [PDF Full-Text (792 KB)] **IEEE CNF**

11 **Towards the implementation of a WCDMA AAA receiver on an FPGA software radio platform**
Korah, S.P.; McDonald, S.A.;
Vehicular Technology Conference, 2001. VTC 2001 Spring. IEEE VTS 53rd , Vol 3 , 6-9 May 2001
Page(s): 1917 -1921 vol.3

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

12 **A run-time support environment for reconfigurable systems**
Bubb, L.; Edwards, M.; Green, P.; Pimlott, C.; Rees, K.; Stewart, M.; Taylor, A. Vakondios, M.; Yates, J.;
Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on , 4-6 Se 2001
Page(s): 135 -141

[Abstract] [PDF Full-Text (568 KB)] **IEEE CNF**

13 **A debug sub-system for embedded-system co-verification**
Liu Jianhua; Zhu Ming; Bian Jinian; Xue Hongxi;
ASIC, 2001. Proceedings. 4th International Conference on , 23-25 Oct. 2001
Page(s): 777 -780

[Abstract] [PDF Full-Text (450 KB)] **IEEE CNF**

14 **Design of a pr cessor to supp rt the teaching of computer systems**
Pearson, M.; Armstrong, D.; McGregor, T.;

Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Workshop on , 29-31 Jan. 2002
Page(s): 240 -244

[Abstract] [PDF Full-Text (397 KB)] **IEEE CNF**

15 **Promises and challenges of evolvable hardware**
Yao, X.; Higuchi, T.;
Systems, Man and Cybernetics, Part C, IEEE Transactions on , Volume: 29 Issu
Feb. 1999
Page(s): 87 -97

[Abstract] [PDF Full-Text (140 KB)] **IEEE JNL**

16 **The LANL Neutron-Science-Center time-of-flight/position-sensitive-module: status and progress**
Rose, C.R.; Hammonds, J.P.; Nelson, R.A.; Weizeorick, J.T.;
Nuclear Science, IEEE Transactions on , Volume: 47 Issue: 2 , April 2000
Page(s): 151 -153

[Abstract] [PDF Full-Text (152 KB)] **IEEE JNL**

17 **Hardware preprocessing for the H1-Level 2 neural network trigger upgrade**
Prevotet, J.-C.; Denby, B.; Fent, J.; Frochtenicht, W.; Garda, P.; Granado, B.; Haberer, W.; Grindhammer, G.; Janauschek, L.; Kiesling, C.; Kobler, I.; Koblitz Nellen, G.; Schmidt, S.; Tzamariudaki, E.; Udluft, S.;
Nuclear Science, IEEE Transactions on , Volume: 49 Issue: 2 , April 2002
Page(s): 362 -368

[Abstract] [PDF Full-Text (345 KB)] **IEEE JNL**

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Your search matched **87** of **950011** documents.

A maximum of **87** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

FPGA and run-time and (reconfigure or reconfiguring o Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Density enhancement of a neural network using FPGAs and run-time reconfiguration**
Eldredge, J.G.; Hutchings, B.L.;
FPGAs for Custom Computing Machines, 1994. Proceedings. IEEE Workshop on 13 April 1994
Page(s): 180 -188

[Abstract] [PDF Full-Text (716 KB)] **IEEE CNF**

2 **RRANN: the run-time reconfiguration artificial neural network**
Eldredge, J.G.; Hutchings, B.L.;
Custom Integrated Circuits Conference, 1994., Proceedings of the IEEE 1994 , May 1994
Page(s): 77 -80

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

3 **A dynamic reconfiguration run-time system**
Burns, J.; Donlin, A.; Hogg, J.; Singh, S.; De Wit, M.;
FPGAs for Custom Computing Machines, 1997. Proceedings., The 5th Annual IE Symposium on , 16-18 April 1997
Page(s): 66 -75

[Abstract] [PDF Full-Text (1008 KB)] **IEEE CNF**

4 **ACEcard™: a high-performance architecture for run-time reconfigura**
Davis, D.; Harris, J.;

Parallel Processing Symposium, 1998. 1998 IPPS/SPDP. Proceedings of the Firs
Merged International...and Symposium on Parallel and Distributed Processing 1
30 March-3 April 1998
Page(s): 616 -619

[Abstract] [PDF Full-Text (420 KB)] **IEEE CNF**

5 **Hardware-software cosynthesis for run-time incrementally reconfigu FPGAs**
Byungil Jeong; Sungjoo Yoo; Sunghyun Lee; Kiyoung Choi;
Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia a
South Pacific , 25-28 Jan. 2000
Page(s): 169 -174

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

6 **Improving functional density using run-time circuit reconfiguration [FPGAs]**
Wirthlin, M.J.; Hutchings, B.L.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: (
Issue: 2 , June 1998
Page(s): 247 -256

[Abstract] [PDF Full-Text (156 KB)] **IEEE JNL**

7 **Run time reconfiguration of FPGA for scanning genomic databases**
Lemoine, E.; Merceron, D.;
FPGAs for Custom Computing Machines, 1995. Proceedings. IEEE Symposium o
21 April 1995
Page(s): 90 -98

[Abstract] [PDF Full-Text (656 KB)] **IEEE CNF**

8 **Fast run-time fault location in dependable FPGA-based applications**
Wei-Je Huang; Mitra, S.; McCluskey, E.J.;
Defect and Fault Tolerance in VLSI Systems, 2001. Proceedings. 2001 IEEE
International Symposium on , 24-26 Oct. 2001
Page(s): 206 -214

[Abstract] [PDF Full-Text (156 KB)] **IEEE CNF**

9 **RRANN: a hardware implementati n f the backpr pagati n algorithı using reconfigurable FPGAs**
Eldredge, J.G.; Hutchings, B.L.;
Neural Networks, 1994. IEEE World Congress on Computational Intelligence., 1 IEEE International Conference on , Volume: 4 , 27 June-2 July 1994
Page(s): 2097 -2102 vol.4

[Abstract] [PDF Full-Text (428 KB)] **IEEE CNF**

10 **Assessing document relevance with run-time reconfigurable machin**
Gunther, B.; Milne, G.; Narasimhan, L.;
FPGAs for Custom Computing Machines, 1996. Proceedings. IEEE Symposium o 19 April 1996
Page(s): 10 -17

[Abstract] [PDF Full-Text (704 KB)] **IEEE CNF**

11 **Modelling and optimising run-time reconfigurable systems**
Luk, W.; Shirazi, N.; Cheung, P.Y.K.;
FPGAs for Custom Computing Machines, 1996. Proceedings. IEEE Symposium o 19 April 1996
Page(s): 167 -176

[Abstract] [PDF Full-Text (624 KB)] **IEEE CNF**

12 **Automating production of run-time reconfigurable designs**
Shirazi, N.; Luk, W.; Cheung, P.Y.K.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium o 17 April 1998
Page(s): 147 -156

[Abstract] [PDF Full-Text (180 KB)] **IEEE CNF**

13 **A design of the new FPGA with data path logic and run time block reconfiguration method**
Jae-Young Kwak; Sang-Sic Yoon; Hung-Jun Kwon; Kwyro Kee;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE Internati Symposium on , Volume: 1 , 30 May-2 June 1999
Page(s): 467 -469 vol.1

[Abstract] [PDF Full-Text (348 KB)] **IEEE CNF**

14 **Using run-time reconfiguration for fault injection in hardware pr to**
Antoni, L.; Leveugle, R.; Feher, B.;
Defect and Fault Tolerance in VLSI Systems, 2000. Proceedings. IEEE Internati
Symposium on , 25-27 Oct. 2000
Page(s): 405 -413

[Abstract] [PDF Full-Text (432 KB)] **IEEE CNF**

15 **Using run-time reconfiguration for fault injection applications**
Antoni, L.; Leveugle, R.; Feher, B.;
Instrumentation and Measurement Technology Conference, 2001. IMTC 2001.
Proceedings of the 18th IEEE , Volume: 3 , 21-23 May 2001
Page(s): 1773 -1777 vol.3

[Abstract] [PDF Full-Text (424 KB)] **IEEE CNF**

16 **The first real operating system for reconfigurable computers**
Wigley, G.; Kearney, D.;
Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceedings. (
Australasian , 29-30 Jan. 2001
Page(s): 130 -137

[Abstract] [PDF Full-Text (740 KB)] **IEEE CNF**

17 **A run-time support environment for reconfigurable systems**
Bubb, L.; Edwards, M.; Green, P.; Pimlott, C.; Rees, K.; Stewart, M.; Taylor, A. Vakondios, M.; Yates, J.;
Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on , 4-6 Se 2001
Page(s): 135 -141

[Abstract] [PDF Full-Text (568 KB)] **IEEE CNF**

18 **Dynamic hardware plugins in an FPGA with partial run-time reconfiguration**
Horta, E.L.; Lockwood, J.W.; Taylor, D.E.; Parlour, D.;
Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002
Page(s): 343 -348

[Abstract] [PDF Full-Text (782 KB)] **IEEE CNF**

19 **An evaluation f an FPGA run-time support system**
Green, P.; Vakondios, M.; Edwards, M.;
Digital System Design, 2002. Proceedings. Euromicro Symposium on , 4-6 Sept

Page(s): 299 -306

[Abstract] [PDF Full-Text (402 KB)] **IEEE CNF**

20 **Netlist partitioning for FPGA-based run-time reconfiguration**
Dueck, S.; Kinsner, W.;
Electrical and Computer Engineering, 2002. IEEE CCECE 2002. Canadian Confer
on , Volume: 2 , 12-15 May 2002
Page(s): 584 -590 vol.2

[Abstract] [PDF Full-Text (698 KB)] **IEEE CNF**

21 **Issues in wireless video coding using run-time-reconfigurable FPGA**
Schoner, B.; Jones, C.; Villasenor, J.;
FPGAs for Custom Computing Machines, 1995. Proceedings. IEEE Symposium o
21 April 1995
Page(s): 85 -89

[Abstract] [PDF Full-Text (592 KB)] **IEEE CNF**

22 **Compilation tools for run-time reconfigurable designs**
Luk, W.; Shirazi, N.; Cheung, P.Y.K.;
FPGAs for Custom Computing Machines, 1997. Proceedings., The 5th Annual IE
Symposium on , 16-18 April 1997
Page(s): 56 -65

[Abstract] [PDF Full-Text (828 KB)] **IEEE CNF**

23 **Handwritten Numeral Recognition Using Personal Handwriting Characteristics Based On Clustering Method**
Yoshinobu Hotta; Satoshi Naoi; Misako Suwa;
Applications of Computer Vision, 1996. WACV '96., Proceedings 3rd IEEE Works
on , 2-4 Dec. 1996
Page(s): 284 -289

[Abstract] [PDF Full-Text (476 KB)] **IEEE CNF**

24 **Visualising rec nfigurable libraries for FPGAs**
Luk, W.; Guo, S.;
Signals, Systems & Computers, 1997. Conference Record of the Thirty-First Asi
Conference on , Volume: 1 , 2-5 Nov. 1997
Page(s): 389 -393 vol.1

[Abstract] [PDF Full-Text (484 KB)] **IEEE CNF**

25 **Incremental reconfiguration for pipelined applications**
Schmit, H.;
FPGAs for Custom Computing Machines, 1997. Proceedings., The 5th Annual IE
Symposium on , 16-18 April 1997
Page(s): 47 -55

[Abstract] [PDF Full-Text (716 KB)] **IEEE CNF**

1 2 3 4 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **6** of **951805** documents.

A maximum of **6** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

FPGA and and (reconfigure or reconfiguring or reconfig Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **The design and implementation of a context switching FPGA**
Scalera, S.M.; Vazquez, J.R.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium o
17 April 1998
Page(s): 78 -85

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

2 **A CAD suite for high-performance FPGA design**
Hutchings, B.; Bellows, P.; Hawkins, J.; Hemmert, S.; Nelson, B.; Rytting, M.;
Field-Programmable Custom Computing Machines, 1999. FCCM '99. Proceeding
Seventh Annual IEEE Symposium on , 21-23 April 1999
Page(s): 12 -24

[Abstract] [PDF Full-Text (188 KB)] **IEEE CNF**

3 **Prototyping of efficient hardware algorithms for data compression in future communication systems**
Mukherjee, A.; Motgi, N.; Becker, J.; Friebe, A.; Habermann, C.; Glesner, M.;
Rapid System Prototyping, 12th International Workshop on, 2001. , 25-27 June
Page(s): 58 -63

[Abstract] [PDF Full-Text (556 KB)] **IEEE CNF**

4 **A run-time support environment f r reconfigurable systems**
Bubb, L.; Edwards, M.; Green, P.; Pimlott, C.; Rees, K.; Stewart, M.; Taylor, A.
Vakondios, M.; Yates, J.;

Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on , 4-6 Se
2001
Page(s): 135 -141

[Abstract] [PDF Full-Text (568 KB)] **IEEE CNF**

5 **A debug sub-system for embedded-system co-verification**
Liu Jianhua; Zhu Ming; Bian Jinian; Xue Hongxi;
ASIC, 2001. Proceedings. 4th International Conference on , 23-25 Oct. 2001
Page(s): 777 -780

[Abstract] [PDF Full-Text (450 KB)] **IEEE CNF**

6 **Promises and challenges of evolvable hardware**
Yao, X.; Higuchi, T.;
Systems, Man and Cybernetics, Part C, IEEE Transactions on , Volume: 29 Issu
Feb. 1999
Page(s): 87 -97

[Abstract] [PDF Full-Text (140 KB)] **IEEE JNL**

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

> Advanced Search

> Search Help/Tips

Sort by: Title Publication **Publication Date** Score

Results 1 - 20 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

1 Gravity: Fast placement for 3-D VLSI 77%
Stefan Thomas Obenaus , Ted H. Szymanski
ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2003
Volume 8 Issue 3

2 Synthesis of saturation arithmetic architectures 77%
G. A. Constantinides , P. Y. K. Cheung , W. Luk
ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2003
Volume 8 Issue 3

3 An algorithm for mapping loops onto coarse-grained reconfigurable architectures 77%
Jong-eun Lee , Kiyoung Choi , Nikil D. Dutt
ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems June 2003
Volume 38 Issue 7

4 Predicting whole-program locality through reuse distance analysis 77%
Chen Ding , Yutao Zhong
ACM SIGPLAN N tices , Pr ceedings f the ACM SIGPLAN 2003 conference n Pr gramming language design and implementati n June 2003
Volume 38 Issue 5

6 Embedded hardware design case studies: Design flow for HW / SW acceleration transparency in the thumbpod secure embedded system 77%
David Hwang , Bo-Cheng Lai , Patrick Schaumont , Kazuo Sakiyama , Yi Fan , Shenglin Yang , Alireza Hodjat , Ingrid Verbauwhede
Proceedings of the 40th conference on Design automation June 2003

7 Compilation techniques for reconfigurable devices: Data communication estimation and reduction for reconfigurable systems 85%
Adam Kaplan , Philip Brisk , Ryan Kastner
Proceedings of the 40th conference on Design automation June 2003

8 Issues in partitioning & design space eploration for codesign: Dynamic hardware/software partitioning: a first approach 84%
Greg Stitt , Roman Lysecky , Frank Vahid
Proceedings of the 40th conference on Design automation June 2003

9 Compilation techniques for reconfigurable devices: Compiler-generated communication for pipelined FPGA applications 77%
Heidi E. Ziegler , Mary W. Hall , Pedro C. Diniz
Proceedings of the 40th conference on Design automation June 2003

10 How application/technology evolutions will shape classical EDA?: System-on-chip beyond the nanometer wall 77%
Philippe Magarshack , Pierre G. Paulin
Proceedings of the 40th conference on Design automation June 2003

11 Tool support for architectural decisions in embedded systems: CoCo: a hardware/software platform for rapid prototyping of code compression technologies 80%
Haris Lekatsas , Jörg Henkel , Srimat Chakradhar , Venkata Jakkula , Murugan Sankaradass
Proceedings of the 40th conference on Design automation June 2003

12 Poster session: Power-aware architectures and circuits for FPGA-based signal processing 77%
Frank Honoré , Ben Calhoun , Anantha Chandrakasan
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

13 Poster session: An automated and power-aware framework for utilization of IP cores in hardware generated from C descriptions targeting FPGAs 77%
Alex Jones , Prith Banerjee
Proceedings f the 2003 ACM/SIGDA eleventh internati nal symposium n Field pr grammable gate arrays February 2003

14 Poster session: Synthetic circuit generation using clustering and iteration 77%
Paul D. Kundarewich , Jonathan Rose
Pr ceedings f the 2003 ACM/SIGDA eleventh internati nal symp sium n Field pr grammable gate arrays February 2003

15 Routing: Stochastic, spatial routing for hypergraphs, trees, and meshes 77%
Randy Huang , John Wawrzynek , André DeHon
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

16 Poster session: An FPGA architecture with built-in error correction capability 77%
P. K. Lala , B. Kiran Kumar
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

17 Poster session: FPGAs in critical hardware/software systems 77%
Adrian J. Hilton J. Adrian J. Hilton , Gemma Townson , Jon G. Hall
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

18 Poster session: On computation and resource management in an FPGA-based computation environment 77%
Soheil Ghiasi , Karlene Nguyen , Elaheh Bozorgzadeh , Majid Sarrafzadeh
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

19 Poster session: Testing for bit error rate in FPGA communication interfaces 77%
Yongquan Fan , Zeljko Zilic
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

20 Poster session: A SC-based novel configurable analog cell 77%
Binlin Guo , Jiarong Tong
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

> Advanced Search

> Search Help/Tips

Sort by: Title Publication **Publication Date** Score

Results 21 - 40 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

21 Routing: PipeRoute: a pipelining-aware router for FPGAs 85%
Akshay Sharma , Carl Ebeling , Scott Hauck
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

22 Novel architectures: A pipelined configurable gate array for embedded processors 82%
Andrea Lodi , Mario Toma , Fabio Campi
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

23 Poster session: Reconfigurable randomized K-way graph partitioning 80%
Fatih Kocan
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

24 Poster session: Application-dependent testing of FPGAs for bridging faults 77%
Mehdi Baradaran Tahoori
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

25 Poster session: A high resolution diagnosis technique for open and short defects in FPGA interconnects 77%

Mehdi Baradaran Tahoori
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

26 Poster session: A four-bit full adder implemented on fast SiGe FPGAs with novel power control scheme 77%
K. Zhou , M. Chu , C. You , J.-R. Guo , Channakeshav , J. Mayega , B. S. Goda , R. P. Kraft , J. F. McDonald
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

27 Poster session: Lattice adaptive filter implementation for FPGA 77%
Zdenek Pohl , Rudolf Matoušek , Jirí Kadlec , Milan Tichý , Miroslav Lícko
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

28 Prototyping, verification, and test: Implementation of BEE: a real-time large-scale hardware emulation engine 82%
Chen Chang , Kimmo Kuusilinna , Brian Richards , Robert W. Brodersen
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

29 Poster session: Design strategies and modified descriptions to optimize cipher FPGA implementations: fast and compact results for DES and triple-DES 77%
Gaël Rouvroy , Francois-Xavier Standaert , Jean-Jacques Quisquater , Jean-Didier Legat
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

30 Poster session: Wireless sensor networks: a power-scalable motion estimation IP for hybrid video coding 77%
Federico Quaglio , Maurzio Martina , Fabrizio Vacca , Guido Masera , Andrea Molino , Gianluca Piccinini , Maurizio Zamboni
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

31 Poster session: A physical retiming algorithm for field programmable gate arrays 77%
Peter Suaris , Dongsheng Wang , Pei-Ning Guo , Nan-Chi Chou
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

32 Poster session: FPGA-based design of an evolutionary controller for collision-free robot navigation 77%
M. A. H. B. Azhar , K. R. Dimond
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

33 Poster session: A single-FPGA implementation of image connected component labelling 77%
K. Benkrid , S. Sukhsawas , D. Crookes , S. Belkacemi
Pr ceedings f the 2003 ACM/SIGDA eleventh internati nal symp sium n Field pr grammable gate arrays February 2003

34 Poster session: Design of a fingerprint system using a hardware/software environment 77%
Lee Vanderlei Bonato , Rolf Fredi Molz , João Carlos Furtado , Marcos Flores Ferräo , Fernando G. Moraes
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

35 Poster session: An estimation and exploration methodology from system-level specifications: application to FPGAs 77%
Sebastien Bilavarn , Guy Gogniat , Jean Luc Philippe
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

36 Poster session: A granularity-based classification model for systems-on-a-chip 77%
Stephan Bingemer , Peter Zipf , Manfred Glesner
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

37 Poster session: Customized regular channel design in FPGAs 77%
Elaheh Bozorgzadeh , Majid Sarrafzadeh
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

38 Poster session: A high-speed successive erasure BCH decoder architecture 77%
Thomas Buerner
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

39 Poster session: A logic based approach to hardware abstraction 77%
K. Benkrid , S. Belkacemi , D. Crookes
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

40 Poster session: Making area-performance tradeoffs at the high level using the AccelFPGA compiler for FPGAs 77%
P. Banerjee , V. Saxena , J. Uribe , M. Haldar , A. Nayak , V. Kim , D. Bagchi , S. Pal , N. Tripathi , R. Anderson
Pr ceedings f the 2003 ACM/SIGDA eleventh international symp sium n Field pr grammable gate arrays February 2003

Results 21 - 40 f 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

> Advanced Search

> Search Help/Tips

Sort by: Title Publication Publication Date Score

Results 41 - 60 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

41 Poster session: FPGA implementation of a fast Hadamard transformer for WCDMA 77%
Sanat Kamal Bahl , Jim Plusquellic
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

42 Poster session: Design framework for the implementation of the 2-D orthogonal discrete wavelet transform on FPGA 77%
A. Benkrid , D. Crookes , K. Benkrid
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

43 Device-level design: Automatic transistor and physical design of FPGA tiles from an architectural specification 77%
Ketan Padalia , Ryan Fung , Mark Bourgeault , Aaron Egier , Jonathan Rose
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

44 Poster session: On hiding latency in reconfigurable systems: the case of merge-sort for an FPGA-based system 77%
Hossam ElGindy , George Ferizis
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

45 Poster session: Implementation of digital fixed-point approximations to continuous-time IIR filters 77%
J. E. Carletta , R. J. Veillette , F. W. Krach , Z. Fang
Pr ceedings f the 2003 ACM/SIGDA eleventh internati nal symp sium n Field pr grammable gate arrays February 2003

46 Poster session: Recursive circuit clustering for minimum delay and area 77%
Mehrdad Eslami Dehkordi , Stephen D. Brown
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

47 Placement: Hardware-assisted simulated annealing with application for fast FPGA placement 94%
Michael G. Wrighton , André M. DeHon
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

48 Poster session: Using FPGAs for data and reorganization engines: preliminary results for spatial pointer-based data structures 77%
Pedro C. Diniz , Joonseok Park
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

49 Poster session: Track placement: orchestrating routing structures to maximize routability 77%
Katherine Compton , Scott Hauck
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

50 Applications: A fully pipelined memoryless 17.8 Gbps AES-128 encryptor 77%
Kimmo U. Järvinen , Matti T. Tommiska , Jorma O. Skyttä
Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

51 Active base stations and nodes for wireless networks 85%
Athanassios Boulis , Paul Lettieri , Mani Srivastava
Wireless Networks January 2003
Volume 9 Issue 1

52 Modeling methodology for integrated simulation of embedded systems 80%
Akos Ledeczi , James Davis , Sandeep Neema , Aditya Agrawal
ACM Transactions on Modeling and Computer Simulation (TOMACS) January 2003
Volume 13 Issue 1

53 XORP: an open platform for network research 77%
Mark Handley , Orion Hodson , Eddie Kohler
ACM SIGCOMM Computer C mmunication Review January 2003
Volume 33 Issue 1

54 Interface specification for reconfigurable components 88%
Satnam Singh
Pr ceedings f the 2002 IEEE/ACM internati nal c nference n C mputer-aided design November 2002

55 Hardware/software partitioning of software binaries 77%
Greg Stitt , Frank Vahid
Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design November 2002

56 Molecular electronics: devices, systems and tools for gigagate, gigabit chips 77%
Michael Butts , Andrée DeHon , Seth Copen Goldstein
Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design November 2002

57 Session S6.2: compilers and program analysis: PACT HDL: a C compiler targeting ASICs and FPGAs with power and performance optimizations 77%
Alex Jones , Debabrata Bagchi , Satrajit Pal , Xiaoyong Tang , Alok Choudhary , Prith Banerjee
Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems October 2002

58 Session S8.2: system synthesis: HW / SW partitioning approach for reconfigurable system design 80%
K. Ben Chehida , M. Auguin
Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems October 2002

59 High level and architectural synthesis: Improving embedded system design by means of HW-SW compilation on reconfigurable coprocessors 85%
José M. Moya , Fernando Rincón , Francisco Moya , Juan Carlos López
Proceedings of the 15th international symposium on System Synthesis October 2002

60 Reconfigurable system: Datapath merging and interconnection sharing for reconfigurable architectures 80%
Nahri Moreano , Guido Araujo , Zhining Huang , Sharad Malik
Proceedings of the 15th international symposium on System Synthesis October 2002

Inc.

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

61 Reconfigurable system: A run-time word-level reconfigurable coarse-grain functional unit for a VLIW processor 80%
Natalino G. Busá , Carles Rodoreda Sala
Proceedings of the 15th international symposium on System Synthesis October 2002

62 Guest editorial 80%
Majid Sarrafzadeh , Rajeev Jayaraman
ACM Transactions on Design Automation of Electronic Systems (TODAES)
October 2002
Volume 7 Issue 4

63 Instruction generation for hybrid reconfigurable systems 87%
R. Kastner , A. Kaplan , S. Ogrenci Memik , E. Bozorgzadeh
ACM Transactions on Design Automation of Electronic Systems (TODAES)
October 2002
Volume 7 Issue 4

64 A search-based bump-and-refit approach to incremental routing for ECO applications in FPGAs 82%
Shantanu Dutt , Vinay Verma , Hasan Arslan
ACM Transacti ns n Design Aut mati n f Electr nic Systems (TODAES)
October 2002
Volume 7 Issue 4

65 Run-time performance optimization of an FPGA-based deduction engine for SAT solvers 93%
Andreas Dandalis , Viktor K. Prasanna
ACM Transacti ns n Design Aut mati n f Electr nic Systems (TODAES)
October 2002
Volume 7 Issue 4

66 Performance-driven placement for dynamically reconfigurable FPGAs 84%
Guang-Ming Wu , Jai-Ming Lin , Yao-Wen Chang
ACM Transactions on Design Automation of Electronic Systems (TODAES)
October 2002
Volume 7 Issue 4

67 Efficient circuit clustering for area and power reduction in FPGAs 77%
Amit Singh , Ganapathy Parthasarathy , Malgorzata Marek-Sadowska
ACM Transactions on Design Automation of Electronic Systems (TODAES)
October 2002
Volume 7 Issue 4

68 Volume rendering: VIZARD II: a reconfigurable interactive volume rendering system 77%
M. Meißner , U. Kanus , G. Wetekam , J. Hirche , A. Ehlert , W. Straßer , M. Doggett , P. Forthmann , R. Proksa
Proceedings of the conference on Graphics hardware 2002 September 2002

69 Partitioning sequential programs for CAD using a three-step approach 80%
Frank Vahid
ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2002
Volume 7 Issue 3

70 Embedded software automation: from specification to binary: Software synthesis from synchronous specifications using logic simulation techniques 77%
Yunjian Jiang , Robert K. Brayton
Proceedings of the 39th conference on Design automation June 2002

71 E-textiles: The wearable motherboard: a framework for personalized mobile information processing (PMIP) 77%
Sungmee Park , Kenneth Mackenzie , Sundaresan Jayaraman
Proceedings of the 39th conference on Design automation June 2002

72 Processors and accelerators for embedded applications: Unlocking the design secrets of a 2.29 Gb/s Rijndael processor 80%
Patrick R. Schaumont , Henry Kuo , Ingrid M. Verbauwhede
Pr ceedings f the 39th c nference n Design aut mati n June 2002

73 Applications of reconfigurable computing: Dynamic hardware plugins in an FPGA with partial run-time reconfiguration 89%
Edson L. Horta , John W. Lockwood , David E. Taylor , David Parlour
Pr ceedings f the 39th c nference n Design aut mation June 2002

74 Designing SoCs for yield improvement: Using embedded FPGAs for SoC yield improvement 82%
Miron Abramovici , Charles Stroud , Marty Emmert
Proceedings of the 39th conference on Design automation June 2002

75 Applications of reconfigurable computing: A reconfigurable FPGA-based readback signal generator for hard-drive read channel simulator 87%
Jinghuan Chen , Jaekyun Moon , Kia Bazargan
Proceedings of the 39th conference on Design automation June 2002

76 Reconfigurable computing: a survey of systems and software 100%
Katherine Compton , Scott Hauck
ACM Computing Surveys (CSUR) June 2002
Volume 34 Issue 2

77 System design methods: analysis and verification: FPGA resource and timing estimation from Matlab execution traces 77%
Per Bjuréus , Mikael Millberg , Axel Jantsch
Proceedings of the tenth international symposium on Hardware/software codesign May 2002

78 System design methods: scheduling advances: Dynamic run-time HW/SW scheduling techniques for reconfigurable architectures 80%
Juanjo Noguera , Rosa M. Badia
Proceedings of the tenth international symposium on Hardware/software codesign May 2002

79 System partitioning and timing analysis: HW/SW partitioning and code generation of embedded control applications on a reconfigurable architecture platform 82%
Massimo Baleani , Frank Gennari , Yunjian Jiang , Yatish Patel , Robert K. Brayton , Alberto Sangiovanni-Vincentelli
Proceedings of the tenth international symposium on Hardware/software codesign May 2002

80 System design methods: scheduling advances: Reconfigurable SoC design with hierarchical FSM and synchronous dataflow model 99%
Sunghyun Lee , Sungjoo Yoo , Kiyoung Choi
Pr ceedings f the tenth internati nal symp sium n Hardware/s ftware c design May 2002

Results 61 - 80 f 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

Sort by: Title Publication **Publication Date** Score

Results 81 - 100 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

81 Invited talks: Hardware acceleration of graphics and imaging algorithms using FPGAs 77%
Pavel Zemcik
Proceedings of the 18th spring conference on Computer graphics April 2002

82 Design Automation: Board-level multiterminal net assignment 77%
Xiaoyu Song , William N. N. Hung , Alan Mishchenko , Malgorzata Chrzanowska-Jeske , Alan Coppola , Andrew Kennings
Proceedings of the 12th ACM Great Lakes Symposium on VLSI April 2002

83 Report of session: language changes for scheduling, modeling and analysis 77%
Andy Wellings , Tullio Vardanega
ACM SIGAda Ada Letters , Proceedings of the 11th international workshop on Real-time Ada workshop April 2002
Volume 22 Issue 4

84 Topics in Physical Design: Temporal logic replication for dynamically reconfigurable FPGA partitioning 77%
Wai-Kei Mak , Evangeline F. Y. Young
Proceedings of the 2002 international symposium on Physical design April 2002

85 Fast placement approaches for FPGAs 77%
Russell Tessier

ACM Transacti ns n Design Automati n f Electr nic Systems (TODAES) April 2002
Volume 7 Issue 2

86 Cellular and Cryptographic Applications: Application of FPGA technology to accelerate the finite-difference time-domain (FDTD) method 80%
Ryan N. Schneider , Laurence E. Turner , Michal M. Okoniewski
Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays February 2002

87 Architecture Analysis and Automation: Automatic layout of domain-specific reconfigurable subsystems for system-on-a-chip 80%
Shawn Phillips , Scott Hauck
Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays February 2002

88 Software for Reconfigurable Systems: Configuration prefetching techniques for partial reconfigurable coprocessor with relocation and defragmentation 94%
Zhiyuan Li , Scott Hauck
Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays February 2002

89 Software for Reconfigurable Systems: Analysis of quasi-static scheduling techniques in a virtualized reconfigurable machine 87%
Yury Markovskiy , Eylon Caspi , Randy Huang , Joseph Yeh , Michael Chu , John Wawrzynek , André DeHon
Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays February 2002

90 Innovative Applications: A dynamically reconfigurable adaptive viterbi decoder 84%
Sriram Swaminathan , Russell Tessier , Dennis Goeckel , Wayne Burleson
Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays February 2002

91 Synthesis, Verification and Test: Timing verification of dynamically reconfigurable logic for the xilinx virtex FPGA series 85%
Ian Robertson , James Irvine , Patrick Lysaght , David Robinson
Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays February 2002

92 The management of applications for reconfigurable computing using an operating system 98%
Grant Wigley , David Kearney
Australian C mputer Science C mmunicati ns , Pr ceedings of the seventh Asia-Pacific c nference n C mputer systems architecture - V lume 6 January

2002
Volume 24 Issue 3

93 Towards nanocomputer architecture 82%
Paul Beckett , Andrew Jennings
Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture - Volume 6 January 2002
Volume 24 Issue 3

94 Synthesis and Design Tools: A compiler framework for mapping applications to a coarse-grained reconfigurable computer architecture 80%
Girish Venkataramani , Walid Najjar , Fadi Kurdahi , Nader Bagherzadeh , Wim Bohm
Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems November 2001

95 Synthesis and Design Tools: Pattern matching in reconfigurable logic for packet classification 87%
Adam Johnson , Kenneth Mackenzie
Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems November 2001

96 Synthesis and Design Tools: A software development tool chain for a reconfigurable processor 77%
Alberto La Rosa , Luciano Lavagno , Claudio Passerone
Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems November 2001

97 Session 3C: Routing architecture and techniques for FPGAs: A search-based bump-and-refit approach to incremental routing for ECO applications in FPGAs 82%
Vinay Verma , Shantanu Dutt
Proceedings of the 2001 IEEE/ACM international conference on Computer-aided aided design November 2001

98 Building a robust software-based router using network processors 77%
Tammo Spalink , Scott Karlin , Larry Peterson , Yitzchak Gottlieb
ACM SIGOPS Operating Systems Review , Proceedings of the eighteenth ACM symposium on Operating systems principles October 2001
Volume 35 Issue 5

99 A quick safari through the reconfiguration jungle 82%
Patrick Schaumont , Ingrid Verbauwhede , Kurt Keutzer , Majid Sarrafzadeh
Proceedings of the 38th conference on Design automation June 2001

100 Integrating scheduling and physical design into a coherent compilation cycle for reconfigurable computing architectures 82%
Kia Bazargan , Seda Ogrenci , Majid Sarrafzadeh

Pr ceedings of the 38th c nference n Design aut mati n June 2001

Results 81 - 100 f 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

> Advanced Search

> Search Help/Tips

Sort by: Title Publication **Publication Date** Score

Results 101 - 120 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

101 Watermarking of SAT using combinatorial isolation lemmas 77%
Rupak Majumdar , Jennifer L. Wong
Proceedings of the 38th conference on Design automation June 2001

102 A framework for object oriented hardware specification, verification, and synthesis 77%
T. Kuhn , T. Oppold , M. Winterholer , W. Rosenstiel , Marc Edwards , Yaron Kashai
Proceedings of the 38th conference on Design automation June 2001

103 Re-configurable computing in wireless 77%
Bill Salefski , Levent Caglar
Proceedings of the 38th conference on Design automation June 2001

104 Speeding up control-dominated applications through microarchitectural customizations in embedded processors 77%
Peter Petrov , Alex Orailoglu
Proceedings of the 38th conference on Design automation June 2001

105 CryptoManiac: a fast flexible architecture for secure communication 77%
Lisa Wu , Chris Weaver , Todd Austin
ACM SIGARCH C mputer Architecture News , Pr ceedings f the 28th annual internati nal symp sium n C mputer architecture May 2001
Volume 29 Issue 2

106 NanoFabrics: spatial computing using molecular electronics 82%
Seth Copen Goldstein , Mihai Budiu
ACM SIGARCH C mputer Architecture News , Pr ceedings f the 28th annual international symposium n C mputer architecture May 2001
Volume 29 Issue 2

107 A systematic approach to software peripherals for embedded systems 77%
D. Lioupis , A. Papagiannis , D. Psihogiou
Proceedings of the ninth international symposium on Hardware/software codesign April 2001

108 An algorithm for synthesis of large time-constrained heterogeneous adaptive systems 80%
ACM Transactions on Design Automation of Electronic Systems (TODAES) April 2001
Volume 6 Issue 2

109 Optimal FPGA module placement with temporal precedence constraints 84%
S. Fekete , E. Köhler , J. Teich
Proceedings of the conference on Design, automation and test in Europe March 2001

110 A decade of reconfigurable computing: a visionary retrospective 95%
R. Hartenstein
Proceedings of the conference on Design, automation and test in Europe March 2001

111 Managing dynamic reconfiguration overhead in systems-on-a-chip design using reconfigurable datapaths and optimized interconnection networks 87%
Z. Huang , S. Malik
Proceedings of the conference on Design, automation and test in Europe March 2001

112 A HW/SW partitioning algorithm for dynamically reconfigurable architectures 80%
J. Noguera , R. Badia
Proceedings of the conference on Design, automation and test in Europe March 2001

113 Interconnect prediction for programmable logic devices 77%
Michael Hutton
Pr ceedings of the 2001 internati nal w rksh p n System-level interconnect predicti n March 2001

114 Run-Time defect tolerance using JBits 85%
Prasanna Sundararajan , Steven A. Guccione


Pr ceedings f the 2001 ACM/SIGDA ninth internati nal symp sium n Field pr grammable gate arrays February 2001

115 Attacking the semantic gap between application programming languages and configurable hardware 82%

Greg Snider , Barry Shackleford , Richard J. Carter
Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays February 2001

116 Evaluation of the streams-C C-to-FPGA compiler: an applications perspective 80%

Jan Frigo , Maya Gokhale , Dominique Lavenier
Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays February 2001

117 A memory coherence technique for online transient error recovery of FPGA configurations 77%

Wei-Je Huang , Edward J. McCluskey
Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays February 2001

118 The effect of reconfigurable units in superscalar processors 77%

Jorge E. Carrillo , Paul Chow
Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays February 2001

119 Coarse grain reconfigurable architecture (embedded tutorial) 93%

Reiner Hartenstein
Proceedings of the conference on Asia South Pacific Design Automation Conference January 2001

120 The first real operating system for reconfigurable computers 98%

Grant Wigley , David Kearney
Australian Computer Science Communications , Proceedings of the 6th Australasian conference on Computer systems architecture January 2001
Volume 23 Issue 4

Results 101 - 120 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

Sort by: Title Publication **Publication Date** Score

Results 121 - 140 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

121 PipeRench implementation of the instruction path coprocessor 77%
Yuan Chou , Pazhani Pillai , Herman Schmit , John Paul Shen
Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture December 2000

122 Architectural support for fast symmetric-key cryptography 77%
Jerome Burke , John McDonald , Todd Austin
Proceedings of the ninth international conference on Architectural support for programming languages and operating systems November 2000
Volume 34 , 28 Issue 5 , 5

123 MemorIES3: a programmable, real-time hardware emulation tool for multiprocessor server design 77%
Ashwini Nanda , Kwok-Ken Mak , Krishnan Sugarvanam , Ramendra K. Sahoo , Vijayaraghavan Soundararajan , T. Basil Smith
Proceedings of the ninth international conference on Architectural support for programming languages and operating systems November 2000
Volume 34 , 28 Issue 5 , 5

124 MemorIES: a programmable, real-time hardware emulation tool for multiprocessor server design 77%
Ashwini Nanda , Kwok-Ken Mak , Krishnan Sugavanam , Ramendra K. Sahoo , Vijayaraghavan Soundararajan , T. Basil Smith
ACM SIGPLAN N tices November 2000
Volume 35 Issue 11

125 Reconfigurable computing and embedded systems: Configuration management in multi-context reconfigurable systems for simultaneous performance and power optimizations 80%
Rafael Maestre , Milagros Fernandez , Fadi J. Kurdahi , Nader Bagherzadeh , Hartej Singh
Proceedings of the 13th international symposium on System synthesis September 2000

126 System design methodologies and experiences: Artificial neural network implementation on a single FPGA of a pipelined on-line backpropagation 77%
Rafael Gadea , Joaquín Cerdá , Franciso Ballester , Antonio Mocholí
Proceedings of the 13th international symposium on System synthesis September 2000

127 System level modeling and verification: Embedded systems verification with FGPA-enhanced in-circuit emulator 77%
M. Meerwein , C. Baumgartner , T. Wieja , W. Glauert
Proceedings of the 13th international symposium on System synthesis September 2000

128 Depth optimal incremental mapping for field programmable gate arrays 77%
Jason Cong , Hui Huang
Proceedings of the 37th conference on Design automation June 2000

129 System design of active basestations based on dynamically reconfigurable hardware 91%
Athanassios Boulis , Mani B. Srivastava
Proceedings of the 37th conference on Design automation June 2000

130 Hardware-software co-design of embedded reconfigurable architectures 80%
Yanbing Li , Tim Callahan , Ervan Darnell , Randolph Harr , Uday Kurkure , Jon Stockwood
Proceedings of the 37th conference on Design automation June 2000

131 Using general-purpose programming languages for FPGA design 82%
Brad L. Hutchings , Brent E. Nelson
Proceedings of the 37th conference on Design automation June 2000

132 Reconfigurable caches and their application to media processing 77%
Parthasarathy Ranganathan , Sarita Adve , Norman P. Jouppi
ACM SIGARCH C mputer Architecture News , Pr ceedings f the 27th annual international symp sium n C mputer architecture May 2000
Volume 28 Issue 2

133 CHIMAERA: a high-performance architecture with a tightly-coupled reconfigurable functional unit 77%
Zhi Alex Ye , Andreas Moshovos , Scott Hauck , Prithviraj Banerjee
ACM SIGARCH C mputer Architecture News , Pr ceedings f the 27th annual international symposium on Computer architecture May 2000
Volume 28 Issue 2

134 Smart Memories: a modular reconfigurable architecture 84%
Ken Mai , Tim Paaske , Nuwan Jayasena , Ron Ho , William J. Dally , Mark Horowitz
ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture May 2000
Volume 28 Issue 2

135 Bidwidth analysis with application to silicon compilation 77%
Mark Stephenson , Jonathan Babb , Saman Amarasinghe
ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2000 conference on Programming language design and implementation May 2000
Volume 35 Issue 5

136 System-level power optimization: techniques and tools 77%
Luca Benini , Giovanni de Micheli
ACM Transactions on Design Automation of Electronic Systems (TODAES) April 2000
Volume 5 Issue 2

137 A benchmark suite for evaluating configurable computing systems---- status, reflections, and future directions 88%
S. Kumar , L. Pires , S. Ponnuswamy , C. Nanavati , J. Golusky , M. Vojta , S. Wadi , D. Pandalai , H. Spaanenberg
Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000

138 A representation for dynamic graphs in reconfigurable hardware and its application to fundamental graph algorithms 77%
Lorenz Huelsbergen
Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000

139 Programmable memory blocks supporting content-addressable memory 77%
Frank Heile , Andrew Leaver , Kerry Veenstra
Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000

140 Tolerating operational faults in cluster-based FPGAs 77%
Vijay Lakamraju , Russell Tessier
Pr ceedings f the 2000 ACM/SIGDA eighth internati nal symp sium n Field pr grammable gate arrays February 2000

Results 121 - 140 f 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

Results 141 - 160 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

141 Factoring large numbers with programmable hardware 82%
Hea Joung Kim , William H. Mangione-Smith
Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000

142 A reconfigurable multi-function computing cache architecture 82%
Hue-Sung Kim , Arun K. Somani , Akhilesh Tyagi
Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays February 2000

143 A scheduling and allocation method to reduce data transfer time by dynamic reconfiguration 80%
Kazuhito Ito
Proceedings of the 2000 conference on Asia and South Pacific design automation January 2000

144 Prototype microprocessor LSI with scheduling support hardware for operating system on multiprocessor system 77%
Naoki Nishimura , Takahiro Sasaki , Tetsuo Hironaka
Pr ceedings f the 2000 c nference n Asia and South Pacific design aut mati n January 2000

145 Hardware-software cosynthesis for run-time incrementally reconfigurable FPGAs 82%


Byungil Jeong , Sungjoo Yoo , Sunghyun Lee , Kiyoung Choi
Pr ceedings f the 2000 c nference n Asia and S uth Pacific design aut mati n January 2000

146 Multiway FPGA partitioning by fully exploiting design hierarchy 80%

Wen-Jong Fang , Allen C.-H. Wu
ACM Transactions on Design Automation of Electronic Systems (TODAES) January 2000
Volume 5 Issue 1

147 An integrated temporal partioning and partial reconfiguration technique for design latency improvement 84%

Satish Ganesan , Ranga Vemuri
Proceedings of the conference on Design, automation and test in Europe January 2000

148 An object oriented design method for reconfigurable computing systems 84%

Martyn Edwards , Peter Green
Proceedings of the conference on Design, automation and test in Europe January 2000

149 A global synchronization network for a non-deterministic simulation architecture 80%

Marc Bumble , Lee Coraor
Proceedings of the 31st conference on Winter simulation: Simulation---a bridge to the future - Volume 2 December 1999

150 Concurrent D-algorithm on reconfigurable hardware 77%

Fatih Kocan , Daniel G. Saab
Proceedings of the 1999 IEEE/ACM international conference on Computer-aided aided design November 1999

151 A clustering- and probability-based approach for time-multiplexed FPGA partitioning 77%

Mango Chia-Tso Chao , Guang-Ming Wu , Iris Hui-Ru Jiang , Yao-Wen Chang
Proceedings of the 1999 IEEE/ACM international conference on Computer-aided aided design November 1999

152 Scalable distributed visualization using off-the-shelf components 77%

Alan Heirich , Laurent Moll
Proceedings of the 1999 IEEE symposium on Parallel visualization and graphics October 1999

153 Technology mapping for FPGAs with nonuniform pin delays and fast interconnections 77%

Jason Cong , Yean-Yow Hwang , Songjie Xu
Pr ceedings f the 36th ACM/IEEE c nference n Design aut mati n

c nference June 1999

154 Reconfigurable computing: what, why, and implications for design automation 85%
André DeHon , John Wawrzynek
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

155 Hardware compilation for FPGA-based configurable computing machines 82%
Xiaohan Zhu , Bill Lin
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

156 Dynamic fault diagnosis on reconfigurable hardware 82%
Fatih Kocan , Daniel G. Saab
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

157 Dynamically reconfigurable architecture for image processor applications 84%
Alexandro M. S. Adário , Eduardo L. Roehe , Sergio Bampi
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

158 Java driven codesign and prototyping of networked embedded systems 90%
Josef Fleischmann , Klaus Buchenrieder , Rainer Kress
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

159 An automated temporal partitioning and loop fission approach for FPGA based reconfigurable synthesis of DSP applications 92%
Meenakshi Kaul , Ranga Vemuri , Sriram Govindarajan , Iyad Ouaiss
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

160 A massively-parallel easily-scalable satisfiability solver using reconfigurable hardware 87%
Miron Abramovici , Jose T. de Sousa , Daniel Saab
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

Inc.

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

Results 161 - 180 of 200 long listing

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

161 Quo Vadis evolvable hardware? 77%
Moshe Sipper , Daniel Mange , Eduardo Sanchez
Communications of the ACM April 1999
Volume 42 Issue 4

162 Field-programmable gate arrays 77%
Pierre Marchal
Communications of the ACM April 1999
Volume 42 Issue 4

163 Software/hardware co-design implementation for fractal image compression 80%
Tai-Chi Lee , Patrick Robinson , Michael Gubody , Erik Henne
Proceedings of the 37th annual Southeast regional conference (CD-ROM) April 1999

164 Instruction set selection for ASIP design 80%
Michael Gschwind
Proceedings of the seventh international workshop on Hardware/software c design March 1999

165 PiSMA: a parallel VSM architecture 82%
Dimitris Lioupis , Andreas Pipis , Maria Smirli , Michael Stefanidakis
Cr ssr ads March 1999

Volume 5 Issue 3

166 Don't Care discovery for FPGA configuration compression 82%
Zhiyuan Li , Scott Hauck
Pr ceedings f the 1999 ACM/SIGDA seventh internati nal symp sium n Field programmable gate arrays February 1999

167 String matching on multicontext FPGAs using self-reconfiguration 94%
Reetinder P. S. Sidhu , Alessandro Mei , Viktor K. Prasanna
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

168 A reconfigurable arithmetic array for multimedia applications 88%
Alan Marshall , Tony Stansfield , Igor Kostarnov , Jean Vuillemin , Brad Hutchings
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

169 Circuit partitioning for dynamically reconfigurable FPGAs 77%
Huiqun Liu , D. F. Wong
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

170 Exploiting early partial reconfiguration of run-time reconfigurable FPGAs in embedded systems design 82%
Byoungil Jeong , Sungjoo Yoo , Kiyoung Choi
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

171 High-performance 2-D FPGA DCTs using polynomial transforms 77%
Chris Dick
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

172 Configuration cloning: exploiting regularity in dynamic DSP architectures 84%
S. R. Park , W. Burleson
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

173 Memory interfacing and instruction specification for reconfigurable processors 80%
Jeffrey A. Jacob , Paul Chow
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field pr grammable gate arrays February 1999

174 Efficient support of hardware debugging through FPGA physical design partitioning 80%
John Lach , William H. Mangione-Smith , Miodrag Potkonjak

Pr ceedings f the 1999 ACM/SIGDA seventh internati nal symp sium n Field pr grammable gate arrays February 1999

175 High-performance low-cost implementation of two-dimensional DCT processor nn FPGA 77%
L. Naviner , J-L. Danger , C. Laurent
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

176 Hardware/software partitioning between microprocessor and reconfigurable hardware 77%
M. Anand , Sanjiv Kapoor , M. Balakrishnan
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

177 Extra-dimensional island-style FPGAs 80%
Herman Schmit
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

178 Configuration caching vs data caching for striped FPGAs 87%
Deepali Deshpande , Arun K. Somani , Akhilish Tyagi
Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays February 1999

179 CORDS: hardware-software co-synthesis of reconfigurable real-time distributed embedded systems 77%
Robert P. Dick , Niraj K. Jha
Proceedings of the 1998 IEEE/ACM international conference on Computer-aided aided design November 1998

180 Network flow based circuit partitioning for time-multiplexed FPGAs 80%
Huiqun Liu , D. F. Wong
Proceedings of the 1998 IEEE/ACM international conference on Computer-aided aided design November 1998

Search Results

Search Results for: **[FPGA <and> (run-time <or> runtime) <and> (reconfigure <or> reconfiguring <or> reconfigurability)<AND>((FPGA))]**
Found **214** of **113,497 searched.**

Warning: Maximum result set of 200 exceeded. Consider refining.

Search within Results

> Advanced Search

> Search Help/Tips

Sort by: **Title** **Publication** **Publication Date** **Score**

Results 181 - 200 of 200 **long listing**

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page

181 Active basestations & nodes for a mobile environment 80%
Athanassios Boulis , Paul Lettieri , Mani B. Srivastava
Proceedings of the 1st ACM international workshop on Wireless mobile multimedia October 1998

182 HiPART: a new hierarchical semi-interactive HW-/SW partitioning approach with fast debugging for real-time embedded systems 77%
Thomas Hollstein , Jürgen Becker , Andreas Kirschbaum , Manfred Glesner
Proceedings of the 6th international workshop on Hardware/software codesign March 1998

183 Configuration prefetch for single context reconfigurable coprocessors 88%
Scott Hauck
Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays March 1998

184 Managing pipeline-reconfigurable FPGAs 87%
Srihari Cadambi , Jeffrey Weener , Seth Copen Goldstein , Herman Schmit , Donald E. Thomas
Pr ceedings of the 1998 ACM/SIGDA sixth internati nal symp sium n Field pr grammable gate arrays March 1998

185 Efficiently supporting fault-tolerance in FPGAs 82%
John Lach , William H. Mangione-Smith , Miodrag Potkonjak

Pr ceedings f the 1998 ACM/SIGDA sixth internati nal symp sium n Field pr grammable gate arrays March 1998

186 Fast module mapping and placement for datapaths in FPGAs 85%

Timothy J. Callahan , Philip Chong , André DeHon , John Wawrzynek
Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays March 1998

187 A hardware/software prototyping environment for dynamically reconfigurable embedded systems 94%

Josef Fleischmann , Klaus Buchenrieder , Rainer Kress
Proceedings of the 6th international workshop on Hardware/software codesign March 1998

188 A method for them embedding of arbitrary communication topologies into configurable parallel computers 77%

Otto Wohlmuth , Friedrich Mayer-Lindenberg
Proceedings of the 1998 ACM symposium on Applied Computing February 1998

189 The road ahead in CPLD & FPGA design methodology (panel) 80%

Rhondalee Rohleder , John Birkner , Don Faria , Steve Golson , Robert K. Beachler , Bruce Kleinman , Mike Dini , Bob Donaldson , Davie Kohlmeier
Proceedings of the 34th annual conference on Design automation conference June 1997

190 Power optimization for FPGA look-up tables 80%

Michael J. Alexander
Proceedings of the 1997 international symposium on Physical design April 1997

191 YARDS: FPGA/MPU hybrid architecture for telecommunication data processing 80%

Akihiro Tsutsui , Toshiaki Miyazaki
Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays February 1997

192 Module generation of complex macros for logic-emulation applications 80%

Wen-Jong Fang , Allen C.-H. Wu , Duan-Ping Chen
Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays February 1997

193 Improving functional density through run-time constant propagation 99%

Michael J. Wirthlin , Brad L. Hutchings
Proceedings of the 1997 ACM fifth international symposium on Field-pr grammable gate arrays February 1997

194 Wormhole run-time reconfiguration 96%

Ray Bittner , Peter Athanas
Pr ceedings f the 1997 ACM fifth internati nal symposium n Field-

pr grammable gate arrays February 1997

195 Serial fault emulation 89%
Luc Burgun , Frédéric Reblewski , Gérard Fenelon , Jean Berbier , Olivier Lepape
Pr ceedings of the 33rd annual c nference n Design aut mation conference June 1996

196 Evaluation of FPGA resources for built-in self-test of programmable logic blocks 80%
Charles Stroud , Ping Chen , Srinivasa Konala , Miron Abramovici
Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays February 1996

197 Fault emulation: a new approach to fault grading 88%
Kwang-Ting Cheng , Shi-Yu Huang , Wei-Jin Dai
Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design December 1995

198 Combining structural and procedural programming by parallelizing compilation 80%
Reiner W. Hartenstein , Karin Schmidt
Proceedings of the 1995 ACM symposium on Applied computing February 1995

199 Hardware assists for high performance computing using a mathematics of arrays 80%
H. Pottinger , W. Eatherton , J. Kelly , T. Schiefelbein , L. R. Mullin , R. Ziegler
Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays February 1995

200 A high-performance microarchitecture with hardware-programmable functional units 80%
Rahul Razdan , Michael D. Smith
Proceedings of the 27th annual international symposium on Microarchitecture November 1994

Results 181 - 200 of 200 **long listing**

Prev Page 1 2 3 4 5 6 7 8 9 10 Next Page